

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|-------------|---|-----------------|------------|
| Applicant: | Yong-Jun Hu | Examiner: | Unknown |
| Serial No.: | Unknown | Group Art Unit: | Unknown |
| Filed: | Herewith | Docket: | 303.098US4 |
| Title: | LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS | | |

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

In the Specification

On page 1, under the title, please add the following paragraph:

—This application is a divisional of U.S. Serial No. 09/139,583 filed August 25, 1998, which is a continuation of U.S. Serial No. 08/964,575 filed November 5, 1997, now U.S. Patent 5,863,393, which is a divisional of U.S. Serial No. 08/677,659 filed July 8, 1996, now U.S. Patent 5,725,739. —

Please substitute the following paragraph that begins on Page 1, line 19 and ends on Page 2, line 5 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

One way in which circuit resistance is decreased is by creating low-resistance, ohmic contacts at the device level. Ohmic contacts exhibit nearly linear current-voltage characteristics in both directions of current flow. Various factors affect the type of contact which is maintained. Increasing dopant concentration in the semiconductor contact area decreases contact resistance, up to the solubility of the dopant at the temperature at which it is introduced. Unclean semiconductor surfaces (i.e., those which contain a native oxide film) increase contact resistance. Native oxides are a problem due to silicon's rapid oxidation rate when exposed to an oxygen

ambient. The most widely used method for removal of such oxides is by dipping the wafer in a hydrofluoric acid solution. However, this does not [provide] perfect cleaning of the semiconductor substrate because some native oxide forms between the time of the hydrofluoric acid dip and the deposition of metal contacts. Sputter etching has been used in an attempt to alleviate this imperfection, but it falls short because more oxide is introduced onto the semiconductor substrate than is removed.

Please substitute the following paragraph that begins on Page 3, line 16 and ends on Page 3, line 22 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A primary method for depositing films by PVD is sputtering. Sputtering is a method by which atoms on a target are displaced to a desired surface, where they form a thin film. One possible solution to the problem of over consumption of silicon in shallow junctions is to use a PVD process to deposit a metal/silicon alloy, like titanium silicide. When [the target material] the deposited material is an alloy, the target is generally a composite target consisting of two or more materials mechanically arranged in a selected ratio, to yield a film of the desired alloy composition.

Please substitute the following paragraph that begins on Page 4, line 12 and ends on Page 4, line 20 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A recess feature is defined by an upper and a lower surface. An alloy is deposited in a recess feature of a semiconductor substrate by sputtering an alloy or composite target onto the semiconductor substrate to form a layer of deposited material on the upper surface. After a period of time, a negative bias voltage is applied to the substrate, initiating a resputtering scheme, which operates simultaneously with the sputtering step. The layer of deposited material is resputtered, to redeposit the layer of deposited material onto the lower surface as a first layer

of resputtered material having a different stoichiometry than that of the deposited material. The resulting recess has improved bottom step coverage, which results in improved ohmic contacts.

Please substitute the following paragraph that begins on Page 6, line 15 and ends on Page 6, line 25 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In one embodiment of the invention, a collimated PVD setup is used to obtain a low grazing angle during resputtering. In a second embodiment of the invention, a long-throw process is used to obtain a low, grazing angle during resputtering. A long-throw process utilizes a non-collimated PVD [tool] apparatus. During a long-throw process, spacing between a target and substrate is so large that only a portion of target material, having a small trajectory angle, with respect to the normal direction of the target, can reach the bottom of a contact hole. Note that in the case of resputtering material overhang, the normal direction of the target (material overhang) is measured, extending radially into the contact hole, in the plane of the substrate. The resulting material deposition rate and bottom step coverage are improved using this embodiment, due to the low energy and low angle mechanisms described previously.

Please substitute the following paragraph that begins on Page 6, line 26 and ends on Page 7, line 5 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In a further embodiment of the invention, a sputtering chamber ambient atmosphere comprises argon and a nitrogen concentration of between approximately 0.1 to 3.0 percent by volume. Furthermore, in yet [a further] another embodiment of the invention, the resputtering step is followed by resputtering of at least one layer of material with a different stoichiometry than that of the first resputtered material layer, to form a "graded" stoichiometry of material

deposited in the contact hole. Using a nitrogen ambient increases the ion-to-neutral ratio, which increases the resputtering rate. Therefore, the resulting material deposition rate and bottom step coverage are improved using this embodiment.

Please substitute the following paragraph that begins on Page 7, line 17 and ends on Page 7, line 18 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

[Figure 3 is] Figures 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

Please substitute the following paragraph that begins on Page 8, line 1 and ends on Page 8, line 4 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

Existing equipment, such as a Varian M2000 PVD [tool] apparatus, is utilized to accomplish better bottom step coverage. The invention does not require purchasing a new deposition [tool] system and training employees on how to use it, saving cost and time in fabricating contacts for semiconductor devices.

Please substitute the following paragraph that begins on Page 9, line 26 and ends on Page 10, line 7 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A process window starts by introducing an inert gas, such as argon, from a gas inlet (not shown here), through region 222 and into the space between the target 236 and substrate 200 to form a plasma 240, and allowing it to stabilize (approximately 5 to 10 seconds), as shown in Figure 2. Placing the gas under low, sub-atmospheric pressure creates the plasma (i.e., a mixture of positively charged gas ions and free electrons). A large negative voltage is then applied to the

target 236, directing the plasma ions 240 to the target 236 and sputtering it, for a period of time, allowing a steady-state to be reached. This time depends on the aspect ratio of the hole and actual [dimension] dimensions of the hole. For example, a contact hole of aspect ratio 4, with a 0.5 micron opening needs 5 seconds to reach this steady-state. However, a time frame of between approximately 0 to 25 seconds may be required, depending on geometries and setup of the PVD tool.

Please substitute the following paragraph that begins on Page 11, line 10 and ends on Page 11, line 26 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In addition, after a subsequent annealing step, such preferential resputtering further decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The [anneal] annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to reduce them to titanium oxide and titanium silicide. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce remaining native oxide. In general, between 30 to 50 angstroms of titanium can reduce approximately 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

Please substitute the following paragraph that begins on Page 11, line 27 and ends on Page 12, line 6 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the [latter most] lattermost factor, [uniformities of] single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

Please substitute the following paragraph that begins on Page 12, line 7 and ends on Page 12, line 19 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In a second embodiment of the invention, a long-throw PVD [setup] apparatus is used to obtain a low grazing angle during resputtering. A Varian M2000 PVD tool, or similar equipment well known to one skilled in the art, is used as shown in Figure 2. However, in this embodiment, the [tool] apparatus is noncollimated because a collimator 234 is not used. Instead of using a collimator, a low grazing angle is obtained due to the large substrate-to-target distance. The target 236 power is applied at less than approximately 18 kW. Higher target power provides for a higher deposition rate. The target power is adjusted, so that the desired deposition rate is obtained. A typical argon flow rate is 25 sccm. The target-to-substrate spacing is approximately 450 millimeters. In general, the target-to-substrate spacing is approximately 2 to 3 times greater than that utilized in a collimated setup, and can range from between 100 to 1,000 millimeters, more or less, depending on the relative geometries of the PVD tool and substrate. The target-to-plasma spacing is adjusted, as is well known to one skilled in the art.

Please substitute the following paragraph that begins on Page 12, line 28 and ends on Page 13, line 16 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

After a steady-state is reached, a steady-state resputter scheme is started to redistribute material 150 overhang at the top corner 118 (upper surface) to the bottom corners (on the lower surface) of the contact hole 152, as shown in Figure 1a. The resputtered material 154 on the lower surface 116 of the contact hole 114 has a stoichiometry different than that of the deposited material 150 at the top corner 118, due to the differential resputtering rates of the alloy/composite constituent elements. This resputter scheme is initiated by varying the substrate 110 bias from voltage source 248. For example, using the current setup and contact hole 114 of aspect ratio 4, the zero bias is switched to a small bias (-15 to -65 Volts). In general, the substrate bias voltage should be less than the lowest sputtering threshold energy of any constituent of the alloy target. The amount of material 150 overhang is compensated with the amount of material 154 resputtered, providing a steady state process. The elements in the target material alloy, or composite, resputter at different rates, due to their different atomic masses, resulting in resputtered material being redistributed to the bottom of the contact hole, having a different stoichiometry than the deposited material on the upper surface of the contact hole. In general, heavier elements of a sputtered species sputter at a faster rate than lighter elements. The bias voltage is adjusted according to the elements present in the alloy or composite.

Please substitute the following paragraph that begins on Page 13, line 28 and ends on Page 14, line 15 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In addition, after a subsequent [anneal] annealing step, such preferential resputtering decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The [anneal] annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP)

techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to form titanium oxide and titanium silicide upon subsequent annealing of the material. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce any remaining native oxide. Typically, between 30 to 50 angstroms of titanium can completely reduce 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

Please substitute the following paragraph that begins on Page 14, line 16 and ends on Page 14, line 24 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the [latter most] lattermost factor, [uniformities of] single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

Please substitute the following paragraph that begins on Page 15, line 3 and ends on Page 15, line 14 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The maximum amount of silicon that is consumed from the substrate 310, as shown in [Figure 3] Figure 3a, is that needed to form titanium silicide in its equilibrium state. For example, titanium silicide has an equilibrium ratio of silicon to titanium of 2.0:1. When the resputtered material has a ratio of silicon to titanium of less than 2.0:1, silicon is consumed from the substrate to bring the ratio of silicon to titanium back to 2.0:1 after deposition. Compared to prior art techniques, since titanium silicide is being deposited instead of titanium, the profile of the substrate 310 does not change significantly during the process of forming a titanium silicide layer 354 thereon. The resulting layer of titanium silicide 354 provides lower contact resistance due to its generally planar shape. Although the resulting structure has been described in terms of a contact hole 314, deposited with titanium silicide 354, other types of materials and structures can be used, as described previously, without departing from the scope of the invention.

Please substitute the following paragraph that begins on Page 16, line 15 and ends on Page 16, line 22 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In another embodiment, creating multiple layers of titanium silicides, with a stoichiometry, of TiSi_x , where $x > 2.0$, improves high temperature stability of titanium silicide by approximately 50 to 150 degrees Celsius, depending on how high a value of x device manufacturing processes can tolerate. However, when desired layers of resputtered material comprise a ratio of [titanium-to-silicon] silicon-to-titanium of greater than 2.0:1, the target material and layer of deposited material must have a ratio of [titanium-to-silicon] silicon-to-titanium of at least as great as that of the largest ratio of [titanium-to-silicon] silicon-to-titanium in the resputtered layers of material.

In the Claims

Cancel claims 1-30 without prejudice and add the following new claims 31-70:

31. A contact hole for a semiconductor device, comprising:
 - a bottom surface of a first material;
 - at least one vertical sidewall of a second material;
 - a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.
32. The contact hole of claim 31 where the third material is an alloy or a composite.
33. The contact hole of claim 32 where the third material contains a refractory metal.
34. The contact hole of claim 32 where the third material is a silicide.
35. The contact hole of claim 32 where the third material is rich in titanium.
36. The contact hole of claim 32 where the stoichiometry of the third material is uniform.
37. The contact hole of claim 31 where the first material is silicon.
38. The contact hole of claim 37 where the third material consumes only a minimal amount of the silicon.
39. A contact hole for a semiconductor device, comprising:
 - a bottom surface of a first material;
 - at least one vertical sidewall of a second material and having a high aspect ratio;
 - a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.

40. The contact hole of claim 39 where a height of the sidewall is at least four times a width of the bottom surface.

41. The contact hole of claim 39 where a width of the bottom surface is equal to or less than about 0.5 micron.

42. The contact hole of claim 39 where the third material is substantially confined to the bottom surface of the hole

43. A contact hole for a semiconductor device, comprising:
a bottom surface of a first material;
at least one vertical sidewall of a second material;
a layer of a third material covering the bottom surface with a thickness variation of less than 50%, the third material including at least two different constituent elements.

44. The contact hole of claim 43 where the thickness variation of the layer is less than about 20%.

45. The contact hole of claim 44 where the thickness variation of the layer is less than about 10%.

46. The contact hole of claim 43 where the planar layer contacts the sidewalls.

47. The contact hole of claim 46 where the planar layer does not extend a substantial distance up the sidewall from the bottom.

48. A contact hole for a semiconductor device, comprising:
a bottom surface of a first material;
at least one vertical sidewall of a second material;

a generally planar layer of a third material covering the bottom surface, the third material having a graded stoichiometry between two different elements.

49. The contact hole of claim 48 where the hole has a high aspect ratio.

50. The contact hole of claim 48 where the first material is silicon.

51. The contact hole of claim 48 where the second material is an insulator.

52. The contact hole of claim 48 where the planar layer contacts the sidewalls.

53. The contact hole of claim 52 where the third material is substantially confined to the bottom of the hole.

54. The contact hole of claim 48 where the third material is a silicide.

55. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one sidewall of an insulating material;

a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.

56. The contact hole of claim 55 where the insulator is an oxide, a nitride, or a glass.

57. The contact hole of claim 55 where the layer of the third material does not extend substantially up the sidewall from the bottom.

58. The contact hole of claim 55 where the third material is a silicide.

59. An integrated circuit, comprising:

- a substrate of a first material;
- an insulator of a second material overlying the substrate;
- multiple contact holes through the insulator to the substrate, each contact hole having at least one sidewall of the second material and a generally planar layer contacting the substrate, the layer including at least two different constituent elements.

60. The integrated circuit of claim 59 where the substrate is silicon.

61. The integrated circuit of claim 59 where the second material is an oxide, a nitride, or a glass.

62. The integrated circuit of claim 59 where the planar layer contacts the sidewalls.

63. The integrated circuit of claim 59 where the layer is planar within 50%.

64. The integrated circuit of claim 63 where the layer is planar within 20%.

65. An integrated circuit, comprising:

- a substrate of a first material;
- an insulator of a second material overlying the substrate;
- multiple contact holes through the insulator to the substrate, each contact hole having at least one sidewall of the second material and a generally planar layer of a silicide contacting the substrate.

66. The integrated circuit of claim 65 where the silicide includes a refractory metal.

67. The integrated circuit of claim 66 where the refractory metal is titanium or cobalt.

68. The integrated circuit of claim 65 where the silicide has a uniform stoichiometry.

69. The integrated circuit of claim 65 where the silicide has at least two different stoichiometries.

70. The integrated circuit of claim 65 where the insulator has a top surface free of the silicide.

REMARKS

The modifications to the Specification numbered 2-6 and 8-22 above were previously entered in the parent patent application Serial No. 08/677,659 in response to an Examiner's Amendment to the Record, Paper #6, mailed September 29, 1997, by Examiner Aaron Weisstuch. The remaining modifications to the Specification represent typographical, grammatical, clerical or editorial modifications, and do not introduce new matter that would be prohibited by 35 USC 132.

The uniform stoichiometry recited in claims 36 and 68 is mentioned, inter alia, on page 7 line 25 of the Specification. Minimal consumption of the substrate by the material of the planar layer is discussed on page 15 line 1. Aspect ratios of the hole, specified in claims 39-41, are found on page 8 lines 11-14. Figs. 3a and 3b show the material in the layer at the bottom of the hole being confined thereto, and not extending substantially up the sidewalls, as recited in claims 42, 47, 53, and 57. Thickness variation of the bottom layer, as recited in claims 43-45 and 63-64, is described on page 14 lines 19-24. That the layer contacts the sidewalls, claims 46 and 52, is

PRELIMINARY AMENDMENT

Serial Number: Unknown

Filing Date: Herewith

Title: LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS

Page 15

Dkt: 303.098US4

found on line 29 of the same page. Different stoichiometries, recited in claims 48 and 69, is found on page 15 lines 19-28. The particular insulator materials of claims 56 and 61 are discussed on page 8 lines 10-11. Removal of the material deposited in the bottoms of the contact holes from other areas of the integrated circuit is mentioned on page 14 lines 25-27.

Respectfully submitted,

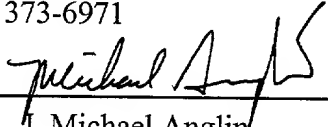
YONG-JUN HU

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6971

Date 5 April 2001

By


J. Michael Anglin

Reg. No. 24,916

"Express Mail" mailing label number: EL671639583US

Date of Deposit: April 5, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 1, LINE 19 ENDING ON PAGE 2, LINE 5**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

One way in which circuit resistance is decreased is by creating low-resistance, ohmic contacts at the device level. Ohmic contacts exhibit nearly linear current-voltage characteristics in both directions of current flow. Various factors affect the type of contact which is maintained. Increasing dopant concentration in the semiconductor contact area decreases contact resistance, up to the solubility of the dopant at the temperature at which it is introduced. Unclean semiconductor surfaces (i.e., those which contain a native oxide film) increase contact resistance. Native oxides are a problem due to silicon's rapid oxidation rate when exposed to an oxygen ambient. The most widely used method for removal of such oxides is by dipping the wafer in a hydrofluoric acid solution. However, this does not perfect cleaning of the semiconductor substrate because some native oxide forms between the time of the hydrofluoric acid dip and the deposition of metal contacts. Sputter etching has been used in an attempt to alleviate this imperfection, but it falls short because more oxide is introduced onto the semiconductor substrate than is removed.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 3, LINE 16 ENDING ON PAGE 3, LINE 22**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

A primary method for depositing films by PVD is sputtering. Sputtering is a method by which atoms on a target are displaced to a desired surface, where they form a thin film. One possible solution to the problem of over consumption of silicon in shallow junctions is to use a PVD process to deposit a metal/silicon alloy, like titanium silicide. When the deposited material is an alloy, the target is generally a composite target consisting of two or more materials mechanically arranged in a selected ratio, to yield a film of the desired alloy composition.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 4, LINE 12 ENDING ON PAGE 4, LINE 20**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

A recess feature is defined by an upper and a lower surface. An alloy is deposited in a recess feature of a semiconductor substrate by sputtering an alloy or composite target onto the semiconductor substrate to form a layer of deposited material on the upper surface. After a period of time, a negative bias voltage is applied to the substrate, initiating a resputtering scheme, which operates simultaneously with the sputtering step. The layer of deposited material is resputtered, to redeposit the layer of deposited material onto the lower surface as a first layer of resputtered material having a different stoichiometry than that of the deposited material. The resulting recess has improved bottom step coverage, which results in improved ohmic contacts.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 15 ENDING ON PAGE 6, LINE 25**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In one embodiment of the invention, a collimated PVD setup is used to obtain a low grazing angle during resputtering. In a second embodiment of the invention, a long-throw process is used to obtain a low, grazing angle during resputtering. A long-throw process utilizes a non-collimated PVD apparatus. During a long-throw process, spacing between a target and substrate is so large that only a portion of target material, having a small trajectory angle, with respect to the normal direction of the target, can reach the bottom of a contact hole. Note that in the case of resputtering material overhang, the normal direction of the target (material overhang) is measured, extending radially into the contact hole, in the plane of the substrate. The resulting material deposition rate and bottom step coverage are improved using this embodiment, due to the low energy and low angle mechanisms described previously.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 26 ENDING ON PAGE 7, LINE 5**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In a further embodiment of the invention, a sputtering chamber ambient atmosphere comprises argon and a nitrogen concentration of between approximately 0.1 to 3.0 percent by volume. Furthermore, in yet another embodiment of the invention, the resputtering step is followed by resputtering of at least one layer of material with a different stoichiometry than that of the first resputtered material layer, to form a "graded" stoichiometry of material deposited in the contact hole. Using a nitrogen ambient increases the ion-to-neutral ratio, which increases the resputtering rate. Therefore, the resulting material deposition rate and bottom step coverage are improved using this embodiment.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 7, LINE 17 ENDING ON PAGE 7, LINE 18**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

[Figure 3 is] Figures 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

Figure 3 is a cross-sectional view of a silicided contact hole formed in accordance with the method of the invention. The contact hole is formed in a substrate 10 and is filled with a silicide material 20. The silicide material 20 is formed by a silicidation process. The contact hole is used for electrical contact to a conductive layer 30. The conductive layer 30 is formed by a conductive material. The contact hole is formed in a substrate 10 and is filled with a silicide material 20. The silicide material 20 is formed by a silicidation process. The contact hole is used for electrical contact to a conductive layer 30. The conductive layer 30 is formed by a conductive material.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 8, LINE 1 ENDING ON PAGE 8, LINE 4**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

Existing equipment, such as a Varian M2000 PVD apparatus, is utilized to accomplish better bottom step coverage. The invention does not require purchasing a new deposition system and training employees on how to use it, saving cost and time in fabricating contacts for semiconductor devices.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
219

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 9, LINE 26 ENDING ON PAGE 10, LINE 7**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

A process window starts by introducing an inert gas, such as argon, from a gas inlet (not shown here), through region 222 and into the space between the target 236 and substrate 200 to form a plasma 240, and allowing it to stabilize (approximately 5 to 10 seconds), as shown in Figure 2. Placing the gas under low, sub-atmospheric pressure creates the plasma (i.e., a mixture of positively charged gas ions and free electrons). A large negative voltage is then applied to the target 236, directing the plasma ions 240 to the target 236 and sputtering it, for a period of time, allowing a steady-state to be reached. This time depends on the aspect ratio of the hole and actual dimensions of the hole. For example, a contact hole of aspect ratio 4, with a 0.5 micron opening needs 5 seconds to reach this steady-state. However, a time frame of between approximately 0 to 25 seconds may be required, depending on geometries and setup of the PVD tool.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 11, LINE 10 ENDING ON PAGE 11, LINE 26**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In addition, after a subsequent annealing step, such preferential resputtering further decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to reduce them to titanium oxide and titanium silicide. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce remaining native oxide. In general, between 30 to 50 angstroms of titanium can reduce approximately 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 11, LINE 27 ENDING ON PAGE 12, LINE 6**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

Clean Version of Specification Paragraph

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 12, LINE 7 ENDING ON PAGE 12, LINE 19**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In a second embodiment of the invention, a long-throw PVD apparatus is used to obtain a low grazing angle during resputtering. A Varian M2000 PVD tool, or similar equipment well known to one skilled in the art, is used as shown in Figure 2. However, in this embodiment, the apparatus is noncollimated because a collimator 234 is not used. Instead of using a collimator, a low grazing angle is obtained due to the large substrate-to-target distance. The target 236 power is applied at less than approximately 18 kW. Higher target power provides for a higher deposition rate. The target power is adjusted, so that the desired deposition rate is obtained. A typical argon flow rate is 25 sccm. The target-to-substrate spacing is approximately 450 millimeters. In general, the target-to-substrate spacing is approximately 2 to 3 times greater than that utilized in a collimated setup, and can range from between 100 to 1,000 millimeters, more or less, depending on the relative geometries of the PVD tool and substrate. The target-to-plasma spacing is adjusted, as is well known to one skilled in the art.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 12, LINE 28 ENDING ON PAGE 13, LINE 16**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

After a steady-state is reached, a steady-state resputter scheme is started to redistribute material 150 overhang at the top corner 118 (upper surface) to the bottom corners (on the lower surface) of the contact hole 152, as shown in Figure 1a. The resputtered material 154 on the lower surface 116 of the contact hole 114 has a stoichiometry different than that of the deposited material 150 at the top corner 118, due to the differential resputtering rates of the alloy/composite constituent elements. This resputter scheme is initiated by varying the substrate 110 bias from voltage source 248. For example, using the current setup and contact hole 114 of aspect ratio 4, the zero bias is switched to a small bias (-15 to -65 Volts). In general, the substrate bias voltage should be less than the lowest sputtering threshold energy of any constituent of the alloy target. The amount of material 150 overhang is compensated with the amount of material 154 resputtered, providing a steady state process. The elements in the target material alloy, or composite, resputter at different rates, due to their different atomic masses, resulting in resputtered material being redistributed to the bottom of the contact hole, having a different stoichiometry than the deposited material on the upper surface of the contact hole. In general, heavier elements of a sputtered species sputter at a faster rate than lighter elements. The bias voltage is adjusted according to the elements present in the alloy or composite.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 13, LINE 28 ENDING ON PAGE 14, LINE 15**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In addition, after a subsequent annealing step, such preferential resputtering decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to form titanium oxide and titanium silicide upon subsequent annealing of the material. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce any remaining native oxide. Typically, between 30 to 50 angstroms of titanium can completely reduce 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

[illegible]

Applicant: Frankie Fariborz Roohparvar

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 15, LINE 3 ENDING ON PAGE 15, LINE 14**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

The maximum amount of silicon that is consumed from the substrate 310, as shown in Figure 3a, is that needed to form titanium silicide in its equilibrium state. For example, titanium silicide has an equilibrium ratio of silicon to titanium of 2.0:1. When the resputtered material has a ratio of silicon to titanium of less than 2.0:1, silicon is consumed from the substrate to bring the ratio of silicon to titanium back to 2.0:1 after deposition. Compared to prior art techniques, since titanium silicide is being deposited instead of titanium, the profile of the substrate 310 does not change significantly during the process of forming a titanium silicide layer 354 thereon. The resulting layer of titanium silicide 354 provides lower contact resistance due to its generally planar shape. Although the resulting structure has been described in terms of a contact hole 314, deposited with titanium silicide 354, other types of materials and structures can be used, as described previously, without departing from the scope of the invention.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 16, LINE 15 ENDING ON PAGE 16, LINE 22**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In another embodiment, creating multiple layers of titanium silicides, with a stoichiometry, of TiSi_x , where $x > 2.0$, improves high temperature stability of titanium silicide by approximately 50 to 150 degrees Celsius, depending on how high a value of x device manufacturing processes can tolerate. However, when desired layers of resputtered material comprise a ratio of silicon-to-titanium of greater than 2.0:1, the target material and layer of deposited material must have a ratio of silicon-to-titanium of at least as great as that of the largest ratio of silicon-to-titanium in the resputtered layers of material.